REMARKS

This is in full and timely response to the above-identified Office Action. The above listing of the claims replaces all prior versions, and listings, of claims in the application. Reexamination and reconsideration in light of the proposed amendments and the following remarks are respectfully requested.

Allowable Subject Matter

The allowance of claims 11 and 13-17, is noted with appreciation.

Rejection under 35 USC § 102

The rejection of claims 9, 10 and 12 as being anticipated by Harper (USP 6,675,316) is respectfully traversed. In this response, it is proposed to amend claims 9, 10 and 12, to clarify the subject matter set forth therein over the structure which is found in Harper.

More specifically, claim 9 has been amended to read:

> A distributed multiprocessing system, comprising:
>
> a fault tolerant external memory unit; and
>
> at least two hosts connected to a network,
>
> wherein each host of the distributed multiprocessing system has a processing unit and an internal memory accessed by the processing unit;
>
> wherein each host further comprises an access device,
>
> wherein each access device is connected to the external memory unit through a respective memory bus, and
>
> wherein each access device is connected with the internal memory of a respective host so that each access device provides a respective processing unit of a respective host with transparent access to the external memory unit via a respective memory bus.

It is submitted that the Harper reference cannot be relied upon to either disclose or suggest such a structure. More specifically, claim 9 as amended, calls for each of the hosts to have an access device and calls for each of the access devices to be connected with the external memory by way of its own (viz., corresponding) memory bus. In addition, claim 9 calls for each of the processing units in each of the hosts to be connected to the external memory device via an access device and its associated bus.

This arrangement is such as to provide each of the processing units in each of the hosts with transparent access to the external memory. This multiple memory bus arrangement, which connects each of multiple access devices with the external memory, at the very least, is not forthcoming from the disclosure of the Harper reference.

Support for the amendments to claim 9 can be found in at least Fig. 1 and the associated written description which is carried in the originally filed specification.

A new claim 18 is added. This claim also finds support in Fig. 1 and the associated written description and is allowable over the art for at least the reason that it sets forth structure which is not found in or suggested by the art of record.

Favorable reconsideration of claims 9, 10 and 12, and allowance of these claims along with the newly presented claim and those which are already allowed, are courteously solicited.

Respectfully submitted,

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